ABSTRACT OF THE DISCLOSURE

A semiconductor device capable of suppressing current concentration in a region where a side surface portion of a lower-level interconnect layer and a via plug which is misaligned with the lower-level interconnect layer are connected, is provided. A lower-level interconnect layer (2) including an anti-reflective film (conductive film) (2b) in a top surface portion thereof is formed on an underlying insulating film (1). An interlayer insulating film (3) is formed so as to cover the lower-level interconnect layer (2) and the underlying insulating film (1). To allow for misalignment between a via plug (4) extending from a top surface of the interlayer insulating film (3) to the lower-level interconnect layer (2) and the lower-level interconnect layer (2), a high resistance layer (5) is provided in a side surface portion of the lower-level interconnect layer (2).